JC03 Rec'd PCT/PTO 15 MAR 2002

dc-304666°FORM PTO-1390 (REV 11-2000) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
449122022900	10/088140 Not yet assigned

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/02441	July 25, 2000	September 16,1999

TITLE OF INVENTION

METHOD FOR MINIMIZING ATM CELL MEMORY

APPLICANT(S) FOR DO/EO/US

Athanase MARIGGIS

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☒ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items: 1) Application Data Sheet; 2) Int'l Search Report; 3) IPER; 4) Return receipt postcard.

CERTIFICATE OF HAND DELIVERY

I hereby certify that this correspondence is being hand filed with the United States Patent and Trademark Office in Washington, D.C. on March 15, 2002.

Melissa Gatton

Melissa Gatton

dc-307166

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY DOCKET NO.
Not yet assigned 10/088140	PCT/DE00/02441	449122022900

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO.....$1,040.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO.....$890.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....$740.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provision of PCT Article 33(1)-(4) $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

	CALCULATIONS PTO USE ONLY	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$0	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	- 20 =		x $18.00	$0	
Independent claims	- 3 =		x $84.00	$0	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$0	

TOTAL OF ABOVE CALCULATIONS =	$890.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by ½.	$0	
SUBTOTAL =	$890.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$0	
TOTAL NATIONAL FEE =	$890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00 per property** +	$40.00	
TOTAL FEES ENCLOSED =	$930.00	
	Amount to be refunded:	**$**
	charged:	**$**

a. ☒ Please charge my **Deposit Account No. 03-1952** (referencing Docket No. 449122022900) in the amount of $930.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

b. ☒ The Commissioner is hereby authorized to charge any additional fees that may be required, or credit any overpayment to **Deposit Account No. 03-1952** (referencing Docket No. 449122022900).

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kevin R. Spivak
Morrison & Foerster LLP
2000 Pennsylvania Avenue, N.W.
Washington, D.C. 20006-1888

SIGNATURE

Kevin R. Spivak
Registration No. 43,148

March 15, 2002

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TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. § 371

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METHOD FOR MINIMIZING ATM CELL MEMORY

APPLICANT(S) FOR DO/EO/US

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CERTIFICATE OF HAND DELIVERY

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Melissa Garton

Melissa Garton

dc-307166

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Melissa Garton

Melissa Garton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Athanase MARIGGIS

Serial No.: Not yet assigned

Filing Date: March 15, 2002

For: METHOD FOR MINIMIZING ATM CELL MEMORY

Examiner: Not yet assigned

Group Art Unit: Not yet assigned

PRELIMINARY AMENDMENT

BOX PCT
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination on the merits, please amend this application as follows:

In the Claims:

Please cancel claims 1-6.

Please add new claims 7-18 as follows:

7. (New) A method for minimizing packet memory, having a multiplicity of channel-specific packet memories, each of which is configured to hold a data packet, comprising:

reading the data packets into a channel-specific packet memory by a writing device; and

removing the data packets from the channel-specific packet memory by a reading device, wherein

the data packets stored in the multiplicity of channel-specific packet memories are read out cyclically under the control of the reading device in accordance with the status of a multiplicity of counting devices.

8. (New) The method as claimed in claim 1, wherein each of the multiplicity of counting devices is assigned to one of the channel-specific packet memories.

9. (New) The method as claimed in claim 1, wherein the status of two of the counting devices differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet and the number of channels.

10. (New) The method as claimed in claim 1, wherein the data packets are ATM cells, and the packet memories are ATM cell memories.

11. (New) The method as claimed in claim 1, wherein the writing device is an interface.

12. (New) The method as claimed in claim 1, wherein the reading device is a framer device which inserts ATM cells into an SDH transmission frame.

13. (New) A system for minimizing packet memory, comprising:

a multiplicity of channel-specific packet memories, each of which is configured to hold a data packet, the data packets being read into a channel-specific packet memory by a writing device and removed from the channel-specific packet memory by a reading device, wherein the data packets stored in the multiplicity of channel-specific packet memories are read out cyclically under the control of the reading device in accordance with the status of a multiplicity of counting devices.

14. (New) The system as claimed in claim 13, wherein each of the multiplicity of counting devices is assigned to one of the channel-specific packet memories.

15. (New) The system as claimed in claim 13, wherein the status of two of the counting devices differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet and the number of channels.

16. (New) The system as claimed in claim 13, wherein the data packets are ATM cells, and the packet memories are ATM cell memories.

17. (New) The system as claimed in claim 13, wherein the writing device is an interface.

18. (New) The system as claimed in claim 13, wherein the reading device is a framer device which inserts ATM cells into an SDH transmission frame.

In the Abstract:

Please replace the Abstract with the substitute Abstract attached hereto.

REMARKS

Amendments to the specification have been made and are submitted herewith in the attached Substitute Specification. We have included both a clean copy of the specification and a marked-up version showing the changes made. The claims and abstract have been amended herewith in the Preliminary Amendment. All amendments have been made to place the application in proper U.S. format and to conform with proper grammatical and idiomatic English. None of the amendments herein are made for reasons related to patentability. No new matter has been added.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 449122022900. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

Dated: March 15, 2002

Kevin R. Spivak
Registration No. 43,148

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Telephone: (202) 887-6924
Facsimile: (202) 263-8396

VERSION WITH MARKINGS TO SHOW CHANGES MADE

For the convenience of the Examiner, the changes made are shown below with deleted text in strikethrough and added text in underline.

In the Claims:

Please cancel claims 1-6.

Please add new claims 7-18 as follows:

7. (New) A method for minimizing packet memory, having a multiplicity of channel-specific packet memories, each of which is configured to hold a data packet, comprising:

reading the data packets into a channel-specific packet memory by a writing device; and

removing the data packets from the channel-specific packet memory by a reading device, wherein

the data packets stored in the multiplicity of channel-specific packet memories are read out cyclically under the control of the reading device in accordance with the status of a multiplicity of counting devices.

8. (New) The method as claimed in claim 1, wherein each of the multiplicity of counting devices is assigned to one of the channel-specific packet memories.

9. (New) The method as claimed in claim 1, wherein the status of two of the counting devices differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet and the number of channels.

10. (New) The method as claimed in claim 1, wherein the data packets are ATM cells, and the packet memories are ATM cell memories.

11. (New) The method as claimed in claim 1, wherein the writing device is an interface.

12. (New) The method as claimed in claim 1, wherein the reading device is a framer device which inserts ATM cells into an SDH transmission frame.

13. (New) A system for minimizing packet memory, comprising:

a multiplicity of channel-specific packet memories, each of which is configured to hold a data packet, the data packets being read into a channel-specific packet memory by a writing device and removed from the channel-specific packet memory by a reading device, wherein the data packets stored in the multiplicity of channel-specific packet memories are read out cyclically under the control of the reading device in accordance with the status of a multiplicity of counting devices.

14. (New) The system as claimed in claim 13, wherein each of the multiplicity of counting devices is assigned to one of the channel-specific packet memories.

15. (New) The system as claimed in claim 13, wherein the status of two of the counting devices differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet and the number of channels.

16. (New) The system as claimed in claim 13, wherein the data packets are ATM cells, and the packet memories are ATM cell memories.

17. (New) The system as claimed in claim 13, wherein the writing device is an interface.

18. (New) The system as claimed in claim 13, wherein the reading device is a framer device which inserts ATM cells into an SDH transmission frame.

In the Abstract:

Please replace the Abstract with the substitute Abstract attached hereto.

METHOD FOR MINIMIZING ATM CELL MEMORY

Abstract

ATM cells are conventionally converted into STM-4 signals as STM-1 datastreams via the Utopia Level 2 interface in the non-concatenated mode, for example for the STM-4 interface. For this purpose, 4 ATM cell memories, which are necessary owing to the specifications of this interface, are required for each channel. In order to reduce this number, the ATM cells are removed from the ATM cell memories with a chronological offset. As a result, the number of ATM cell memories can be halved without restrictions having to be accepted in the transmission process.

METHOD FOR MINIMIZING ATM CELL MEMORY

CLAIM FOR PRIORITY

This application claims priority to International Application No. PCT/DE00/02441 which was published in the German language on July 25, 2000.

TECHNICAL FIELD OF THE INVENTION

The invention relates to a method of minimizing packet memory, and in particular, to minimizing packet memory of multiple channel-specific memories, each of which hold a data packet.

BACKGROUND OF THE INVENTION

Contemporary transmission methods are generally divided into transmission methods which transmit information according to a synchronous transfer mode (STM) or asynchronous transfer mode (ATM).

The synchronous transfer mode STM is based on the transmission of information using SDH (synchronous digital hierarchy) transmission technology. The information is transmitted in transmission frames. These are divided into a control field (SOH, Section Overhead, POH, Path Overhead) and a container field. In the former, control information relating to the connection is transmitted, while in the latter payload data are stored. ATM cells, for example in ATM systems by means of SDH, can also be used as payload data. The data must then be inserted into the frame structure at the start of the transmission process (downstream direction) and removed again at the reception end (upstream direction). For example information relating to the security of the transmission, bit errors, line failure, clock accuracy etc. are possible as control information.

The control field has two subregions SOH and POH. The subregion designated by SOH has control information relating to a transmission section (for example between two switching devices), while control information is transmitted between two users (end-to-end) in the subregion which is designated by POH.

In contemporary synchronous transmission methods, STM-1 interfaces are used. An STM-1 interface is represented physically by a connection between two SDH switching devices. The STM-1 interface is thus the basis of the SDH transmission. For this reason, the SDH switching matrices arranged in the SDH switching device are currently configured in the prior art for the switching through of STM-1 signals.

However, future transmission method contemplate higher-order signals such as STM-N (N>1) signals to be capable of being switched through. Since this is not presently the case, through-switching problems are experienced with the SDH switching matrices which have been used hitherto. A method of avoiding these problems known in the prior art is the virtual concatenated mode. It is a standardized method in which, for example, an STM-4 datastream is split up into 4 STM-1 datastreams. During the transmission, 4 STM-1 datastreams are fed to the receiving switch, switched through and then combined again to form an STM-4 datastream. However, for this purpose, the STM-1 datastreams which are transmitted in channels must have a common reference variable so that later recombination can occur.

The non-concatenated mode is in contrast to the above. Here, the respective signals, for example STM-1 datastreams, are transmitted in channels which are independent of one another.

The standard interface for the transfer of ATM cells in the non-concatenated mode is the Utopia Level 2 interface. ATM cells are received by this interface and written into channel-specific memories in accordance with the assigned channel number. First, it is determined whether the channel-specific memory in question is free. Only if this is the case is an ATM cell written in.

The ATM cells stored in the channel-specific memories are then received by a framer device and inserted into an SDH frame structure. The ATM cells are written at a predefined speed into channel-specific memories and removed again from them with a speed which deviates therefrom. Although the writing-in speed which is predefined by the Utopia Level 2 interface is higher (on average approximately 4 times) than the reading-out speed predefined by the framer device, it should be noted that the writing-in process is stopped by the reception of an SOH field. An increase in the reading-out speed of the framer device is thus absolutely necessary. In this case, the Utopia Level 2 interface may no longer be capable of appropriately filling the the FIFO cell memories of each channel-specific memory. As a consequence, empty cells are inserted into the frame structure, which is to be avoided for considerations of dynamics because this prevents a full load from being reached.

In the prior art, a structure in which a total of 4 FIFO cell memories are used per channel-specific memory has become the solution to this problem. However, neither the framer device nor the Utopia Level 2 interface can simultaneously access the same FIFO cell memory. At the start, all the FIFO cell memories are filled with ATM cells. First, the framer device simultaneously reads out the ATM cells of, in each case, one of the 4 FIFO cell memories of all the

channel-specific memories. As a result, the Utopia Level 2 interface is indirectly actuated in such a way that the FIFO cell memories which are now emptied are filled again with ATM cells by the interface. The framer device then cyclically reads out the further FIFO cell memories. Because a total of 4 FIFO cell memories are provided per channel-specific memory, care is taken to ensure that one of the 4 FIFO cell memories per channel-specific memory is always full. The STM-4 interface then operates at full load. The 4 FIFO cell memories per channel-specific memory average the pauses between the different frequencies during the writing and reading processes.

When there are higher-order interfaces (for example STM-4, STM-16 etc.), the number of FIFO cell memories rises drastically. This results in problems not only with the complexity of the entire transmission system (for example increased susceptibility to faults) but also with an increased power drain of the modules in the interfaces and associated warming. Furthermore, it is associated with increased costs (additional silicon costs).

SUMMARY OF THE INVENTION

In one embodiment of the invention, there is a method for minimizing packet memory, having a multiplicity of channel-specific packet memories, each of which is configured to hold a data packet. The method includes, for example, reading the data packets into a channel-specific packet memory by a writing device and removing the data packets from the channel-specific packet memory by a reading device, wherein the data packets stored in the multiplicity of channel-specific packet memories are read out cyclically under

the control of the reading device in accordance with the status of a multiplicity of counting devices.

In another aspect of the invention, each of the multiplicity of counting devices is assigned to one of the channel-specific packet memories.

In another aspect of the invention, the status of two of the counting devices differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet and the number of channels.

In yet another aspect of the invention, the data packets are ATM cells, and the packet memories are ATM cell memories.

In another aspect of the invention, the writing device is an interface.

In another aspect of the invention, the reading device is a framer device which inserts ATM cells into an SDH transmission frame.

In another embodiment of the invention, there is a system for minimizing packet memory. The system includes, for example, a multiplicity of channel-specific packet memories, each of which is configured to hold a data packet, the data packets being read into a channel-specific packet memory by a writing device and removed from the channel-specific packet memory by a reading device, wherein the data packets stored in the multiplicity of channel-specific packet memories are read out cyclically under the control of the reading device in accordance with the status of a multiplicity of counting devices.

In another aspect of the invention, each of the multiplicity of counting devices is assigned to one of the channel-specific packet memories.

In another aspect of the invention, the status of two of the counting devices differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet and the number of channels.

In still another aspect of the invention, the data packets are ATM cells, and the packet memories are ATM cell memories.

In another aspect of the invention, the writing device is an interface.

In another aspect of the invention, the reading device is a framer device which inserts ATM cells into an SDH transmission frame.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is explained in more detail below with reference to an exemplary embodiment. In the drawings:

Fig. 1 shows the circuit arrangement according to the invention in a communications system.

Fig. 2 shows the circuit arrangement according to the invention.

Fig. 3 shows the conditions on the data lines Data_Ch0... Data_Ch3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention indicates a way in which the number of cell memories for the non-concatenated mode can be reduced.

One advantage of the invention is the spatial arrangement of the FIFO cell memories of the prior art is converted, as it were, into a chronological arrangement. This means that the definition of the

Utopia Level 2 interface is taken into account by ensuring that if the reading device accesses an ATM cell memory, an ATM cell is stored in it, and it is thus not necessary to insert any empty cells into the SDH transmission frame. This is achieved by virtue of the fact that the ATM cells stored in the ATM cell memory are removed from them in a chronologically staggered reading-out process.

Fig. 1 shows the circuit arrangement according to the invention in a communications system KS. According to the arrangement, a switching matrix SN, which can be used for switching through the ATM cells, is disclosed as a central component of the communications system KS. In addition, ATM port devices P and devices SDH, between which the Utopia Level 2 interface is arranged, are shown. The interface is simultaneously part of the two devices. The circuit arrangement according to the invention is then integrated into the device SDH. Framer devices (not shown here in more detail) which integrate the ATM cells into SDH transmission frames are to be considered as part of the device SDH. The circuit arrangement according to the invention is located in the downstream direction.

Fig. 2 shows the circuit arrangement according to the invention in detail. According to said arrangement, channel-specific memories SP0...SP3 which each have 2 FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ are disclosed. An FIFO cell memory can hold precisely one ATM cell. 2 FIFO cell memories are necessary because writing/reading processes cannot be performed simultaneously in one ATM cell memory. Therefore, while one ATM cell is removed from one of the ATM cell memories, a further ATM cell can thus be written into the remaining ATM cell memory.

According to Fig. 2, the channel-specific memory SP0 thus has the two FIFO cell memories $FIFO_{01}$, $FIFO_{02}$, the

channel-specific memory SP1 has the two FIFO cell memories $FIFO_{11}$, $FIFO_{12}$ and so on. The channel-specific memories SP0...SP3 are operatively connected to the Utopia Level 2 interface. The interface receives the ATM cells from the ATM port P and writes them to one of the two FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ of the respective channel-specific memory SP0...SP3 in accordance with the channel Ch0...Ch3. The channel Ch0 is thus assigned the channel-specific memory SP0, and the channel Ch1 is thus assigned the channel-specific memory SP1 etc. The Utopia Level 2 interface ensures that the ATM cell memories are filled with ATM cells. The reason for this is that otherwise the framer device integrates empty cells into the SDH frames. The ATM cells are written into the channel-specific memories at a speed which is predefined by the Utopia Level 2 interface.

Furthermore, Fig. 2 shows a framer device FR. It removes the ATM cells from one of the two FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ of the respective channel-specific memory SP0...SP3 and integrates them into SDH transmission frames. The reading-out processes are supported by a reading counter RC which controls the chronological sequencing of the reading-out processes by means of devices RC0...RC3. The ATM cells are removed from the respective channel-specific memories SP0...SP3 again at a speed which differs from the writing-in speed and is predefined by the framer device FR.

In order to aim at transmission of the greatest possible efficiency, the Utopia Level 2 interface fills up the channel-specific memories SP0...SP3 with ATM cells, and the framer device FR must correspondingly read out the ATM cells, in such a way that the dwell time of the ATM cells in the FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ is as short as possible. For this purpose, the

writing/reading processes have to be correspondingly matched to one another.

For this purpose, the writing/reading process is started from an initial state. In this state, the FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ are to be filled with ATM cells. The Utopia Level 2 interface thus writes no ATM cells into the channel-specific memories SP0...SP3. The framer device FR initially reads out an ATM cell from the ATM cell memory $FIFO_{01}$ of the channel-specific memory SP0 byte by byte. The decisive factor here is the counter reading of the counting device RC0. The counter reading results from the counting device RC being acted on by an offset. In the present case, this offset is 0 bytes.

The counter reading of the counting device RC1 then specifies when the ATM cell stored in the ATM cell memory $FIFO_{11}$ of the channel-specific memory SP1 is to be read out. The counter reading results from the counting device RC being acted on by a further offset. In the present case, this is 13 bytes. This means that the reading out of the ATM cell stored in the cell memory $FIFO_{11}$ is not started until 13 bytes of the ATM cell of the ATM cell memory $FIFO_{01}$ have been read out. The offsets of the counting devices RC2 and RC3 are 26 and 39 bytes. The reading out takes place cyclically. During the reading-out processes, the Utopia Level 2 interface can write further ATM cells into the ATM cell memories. The criterion for this is, however, that the respective ATM cell memory is empty. As a result of this method, 4 cell memories do not empty simultaneously as in the prior art but rather the cell memories empty sequentially (see Fig. 3). As a result, only 2 ATM cell memories per channel-specific memory are required.

Fig. 3 shows the conditions on the data lines Data_Ch0...Data_Ch3 downstream of the channel-specific memories SP0...SP3. The ATM cells are indicated by header H and payload P. The chronological offset of the transmission is clearly apparent here.

In the exemplary embodiment, the minimization of the ATM cell memories was referred to. However, the invention is not restricted to ATM cells and ATM cell memories. Instead, packets of a general type such as IP packets, for example, can also be removed from packet memories in accordance with the method according to the invention. As a consequence, the packet memories can then be minimized in the same way as the ATM cell memories of the exemplary embodiment.

Substitute Specification (Marked-up Version)

~~Description~~

METHOD FOR MINIMIZING ATM CELL MEMORY

CLAIM FOR PRIORITY

This application claims priority to International Application No. PCT/DE00/02441 which was published in the German language on July 25, 2000.

TECHNICAL FIELD OF THE INVENTION

The invention relates to a method ~~according to the preamble of patent claim 1.~~ **of minimizing packet memory, and in particular, to minimizing packet memory of multiple channel-specific memories, each of which hold a data packet.**

BACKGROUND OF THE INVENTION

Contemporary transmission methods are generally divided into transmission methods which transmit information according to a synchronous transfer mode (STM) or asynchronous transfer mode (ATM).

The synchronous transfer mode STM is based on the transmission of information using SDH (synchronous digital hierarchy) transmission technology. ~~Here, the~~ ~~to~~ **The** information is transmitted in transmission frames. These are divided into a control field (SOH, Section Overhead~~,~~ **,** POH, Path Overhead) and a container field. In the former, control information relating to the connection is transmitted, while in the latter payload data are stored. ATM cells, for example in ATM systems by means of SDH, can also be used ~~here~~ as payload data. ~~Said~~ **The** data must then be inserted into the frame structure at the start of the transmission process (downstream direction) and removed again at the reception end (upstream direction). For example information relating to the security of the transmission, bit errors, line failure, clock accuracy

etc. are possible as control information.

The control field has two subregions SOH and POH. The subregion designated by SOH has control information relating to a transmission section (for example between two switching devices), while control information is transmitted between two users (end-to-end) in the subregion which is designated by POH.

In contemporary synchronous transmission methods, STM-1 interfaces are used. An STM-1 interface is represented physically by a connection between two SDH switching devices. The STM-1 interface is thus the basis of the SDH transmission. For this reason, the SDH switching matrices arranged in the SDH switching device are currently configured in the prior art for the switching through of STM-1 signals.

However, ~~in future the intention is for~~ **future transmission method contemplate** higher-order signals such as STM-N (N>1) signals to be capable of being switched through. ~~Because~~ **Since** this is not **presently** the case ~~at present~~, through-switching problems are experienced with the SDH switching matrices which have been used hitherto. A method of avoiding these problems ~~which has been~~ known in the prior art is the virtual concatenated mode. It is a standardized method ~~with~~ **in** which, for example, an STM-4 datastream is split up into 4 STM-1 datastreams. During the transmission, 4 STM-1 datastreams are ~~thus~~ fed to the receiving switch, switched through and then combined again to form an STM-4 datastream. However, for this purpose, the STM-1 datastreams which are transmitted in channels must have a common reference variable so that later recombination can occur.

The non-concatenated mode is ~~to be seen~~ in contrast to the above. Here, the respective signals, for example STM-1 datastreams, are transmitted in channels which

are independent of one another.

The standard interface for the transfer of ATM cells in the non-concatenated mode is the Utopia Level 2 interface. ATM cells are received by this interface and written into channel-specific memories in accordance with the assigned channel number. ~~In a first step~~ **First**, it is determined ~~here~~ whether the channel-specific memory in question is free. Only if this is the case is an ATM cell written in.

The ATM cells stored in the channel-specific memories are then received by a framer device and inserted into an SDH frame structure. The ATM cells are ~~thus~~ written at a predefined speed into channel-specific memories and removed again from them with a speed which deviates therefrom. Although the writing-in speed which is predefined by the Utopia Level 2 interface is higher (on average approximately 4 times) than the reading-out speed predefined by the framer device, it ~~is to be borne in mind here~~ **should be noted** that the writing-in process is stopped by the reception of an SOH field. An increase in the reading-out speed of the framer device is thus absolutely necessary. In this case, the Utopia Level 2 interface may no longer be capable of appropriately filling the the FIFO cell memories of each channel-specific memory. As a consequence, empty cells are inserted into the frame structure, which is to be avoided for considerations of dynamics because this prevents a full load from being reached.

In the prior art, a structure in which a total of 4 FIFO cell memories are used per channel-specific memory has become ~~apparent as~~ the solution to this problem. ~~Here, it is necessary to bear in mind that~~ **However,** neither the framer device nor the Utopia Level 2 interface can simultaneously access the same FIFO cell memory. At the start, all the FIFO cell memories are

filled with ATM cells. ~~In a first step~~ **First**, the framer device simultaneously reads out the ATM cells of, in each case, one of the 4 FIFO cell memories of all the channel-specific memories. As a result, the Utopia Level 2 interface is indirectly actuated in such a way that the FIFO cell memories which are now emptied are filled again with ATM cells by ~~said~~ **the** interface. The framer device then cyclically reads out the further FIFO cell memories. Because a total of 4 FIFO cell memories are provided per channel-specific memory, care is taken to ensure that one of the 4 FIFO cell memories per channel-specific memory is always full. The STM-4 interface then operates at full load. The 4 FIFO cell memories per channel-specific memory average the pauses between the different frequencies during the writing and reading processes.

~~It is problematic here that when~~ **When** there are higher-order interfaces (for example STM-4, STM-16 etc.), the number of FIFO cell memories rises drastically. ~~However, this~~ **This** results in problems not only with the complexity of the entire transmission system (for example increased susceptibility to faults) but also with an increased power drain of the modules in the interfaces and associated warming. Furthermore, it is associated with increased costs (additional silicon costs).

~~The invention is based on the object of indicating a way in which the number of cell memories for the non-concatenated mode can be reduced.~~

SUMMARY OF THE INVENTION

In one embodiment of the invention, there is a method for minimizing packet memory, having a multiplicity of channel-specific packet memories, each of which is configured to hold a data packet. The

method includes, for example, reading the data packets into a channel-specific packet memory by a writing device and removing the data packets from the channel-specific packet memory by a reading device, wherein the data packets stored in the multiplicity of channel-specific packet memories are read out cyclically under the control of the reading device in accordance with the status of a multiplicity of counting devices.

In another aspect of the invention, each of the multiplicity of counting devices is assigned to one of the channel-specific packet memories.

In another aspect of the invention, the status of two of the counting devices differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet and the number of channels.

In yet another aspect of the invention, the data packets are ATM cells, and the packet memories are ATM cell memories.

In another aspect of the invention, the writing device is an interface.

In another aspect of the invention, the reading device is a framer device which inserts ATM cells into an SDH transmission frame.

In another embodiment of the invention, there is a system for minimizing packet memory. The system includes, for example, a multiplicity of channel-specific packet memories, each of which is configured to hold a data packet, the data packets being read into a channel-specific packet memory by a writing device and removed from the channel-specific packet memory by a reading device, wherein the data packets stored in the multiplicity of channel-specific packet memories

are read out cyclically under the control of the reading device in accordance with the status of a multiplicity of counting devices.

In another aspect of the invention, each of the multiplicity of counting devices is assigned to one of the channel-specific packet memories.

In another aspect of the invention, the status of two of the counting devices differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet and the number of channels.

In still another aspect of the invention, the data packets are ATM cells, and the packet memories are ATM cell memories.

In another aspect of the invention, the writing device is an interface.

In another aspect of the invention, the reading device is a framer device which inserts ATM cells into an SDH transmission frame.

~~The invention is achieved on the basis of the features specified in the preamble of patent claim 1 by means of the features claimed in the characterizing part.~~

~~An advantage of the invention is in particular the fact that the spatial arrangement of the FIFO cell memories of the prior art is converted, as it were, into a chronological arrangement. This means that, here too, the definition of the Utopia Level 2 interface is taken into account by ensuring that if the reading device accesses an ATM cell memory, an ATM cell is always stored in it, and it is thus not necessary to insert any empty cells into the SDH transmission frame. This is achieved by virtue of the fact that the ATM cells stored in the ATM cell memory are removed from them in~~

~~a chronologically staggered reading out process. Advantageous developments of the invention are specified in the subclaims.~~

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is explained in more detail below with reference to an exemplary embodiment. In the ~~drawing~~ **drawings**:

Fig. 1 shows the ~~arrangement of the~~ circuit arrangement according to the invention in a communications system~~,~~**.**

Fig. 2 shows the circuit arrangement according to the invention~~,~~**.**

Fig. 3 shows the conditions on the data lines Data_Ch0... Data_Ch3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention indicates a way in which the number of cell memories for the non-concatenated mode can be reduced.

One advantage of the invention is the spatial arrangement of the FIFO cell memories of the prior art is converted, as it were, into a chronological arrangement. This means that the definition of the Utopia Level 2 interface is taken into account by ensuring that if the reading device accesses an ATM cell memory, an ATM cell is stored in it, and it is thus not necessary to insert any empty cells into the SDH transmission frame. This is achieved by virtue of the fact that the ATM cells stored in the ATM cell memory are removed from them in a chronologically staggered reading-out process.

Fig. 1 shows the ~~Fig. 1 shows the arrangement of the~~

circuit arrangement according to the invention in a communications system KS. According to ~~said~~ **the** arrangement, a switching matrix SN, which can be used for switching through the ATM cells, is disclosed as a central component of the communications system KS. In addition, ATM port devices P and devices SDH, between which the Utopia Level 2 interface is arranged, are shown. ~~Said~~ **The** interface is simultaneously part of the two devices. The circuit arrangement according to the invention is then integrated into the device SDH. Framer devices (not shown here in more detail) which integrate the ATM cells into SDH transmission frames are to be considered as part of the device SDH. The circuit arrangement according to the invention is located in the downstream direction.

Fig. 2 shows the circuit arrangement according to the invention in detail. According to said arrangement, channel-specific memories SP0...SP3 which each have 2 FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ are disclosed. An FIFO cell memory can hold precisely one ATM cell. 2 FIFO cell memories are necessary because writing/reading processes cannot be performed simultaneously in one ATM cell memory. Therefore, while one ATM cell is removed from one of the ATM cell memories, a further ATM cell can thus be written into the remaining ATM cell memory.

According to Fig. 2, the channel-specific memory SP0 thus has the two FIFO cell memories $FIFO_{01}$, $FIFO_{02}$, the channel-specific memory SP1 has the two FIFO cell memories $FIFO_{11}$, $FIFO_{12}$ and so on. The channel-specific memories SP0...SP3 are operatively connected to the Utopia Level 2 interface. ~~Said~~ **The** interface receives the ATM cells from the ATM port P and writes them to one of the two FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ of the respective channel-specific memory SP0...SP3 in accordance with the channel Ch0...Ch3. The channel Ch0 is thus assigned the channel-specific memory SP0, and the

channel Ch1 is thus assigned the channel-specific memory SP1 etc. The Utopia Level 2 interface ~~must ensure at all times~~ **ensures** that the ATM cell memories are filled with ATM cells. The reason for this is that otherwise the framer device integrates empty cells into the SDH frames. The ATM cells are written into the channel-specific memories at a speed which is predefined by the Utopia Level 2 interface.

Furthermore, Fig. 2 shows a framer device FR. It removes the ATM cells from one of the two FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ of the respective channel-specific memory SP0...SP3 and integrates them into SDH transmission frames. The reading-out processes are supported by a reading counter RC which controls the chronological sequencing of the reading-out processes by means of devices RC0...RC3. The ATM cells are removed from the respective channel-specific memories SP0...SP3 again at a speed which differs from the writing-in speed and is predefined by the framer device FR.

In order to aim at transmission of the greatest possible efficiency, the Utopia Level 2 interface ~~must fill~~ **fills** up the channel-specific memories SP0...SP3 with ATM cells, and the framer device FR must correspondingly read out the ATM cells, in such a way that the dwell time of the ATM cells in the FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ is as short as possible. For this purpose, the writing/reading processes have to be correspondingly matched to one another.

For this purpose, the writing/reading process is started from an initial state. In this state, ~~all~~ the FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ are to be filled with ATM cells. The Utopia Level 2 interface thus writes no ATM cells into the channel-specific memories SP0...SP3. The framer device FR initially reads out an ATM cell from the ATM cell memory $FIFO_{01}$ of the channel-specific

memory SP0 byte by byte. The decisive factor here is the counter reading of the counting device RC0. The counter reading results from the counting device RC being acted on by an offset. In the present case, this offset is 0 bytes.

The counter reading of the counting device RC1 then specifies when the ATM cell stored in the ATM cell memory $FIFO_{11}$ of the channel-specific memory SP1 is to be read out. The counter reading results from the counting device RC being acted on by a further offset. In the present case, this is 13 bytes. This means that the reading out of the ATM cell stored in the cell memory $FIFO_{11}$ is not started until 13 bytes of the ATM cell of the ATM cell memory $FIFO_{01}$ have been read out. The offsets of the counting devices RC2 and RC3 are 26 and 39 bytes. The reading out takes place cyclically. During the reading-out processes, the Utopia Level 2 interface can write further ATM cells into the ATM cell memories. The criterion for this is, however, that the respective ATM cell memory is empty. As a result of this method, 4 cell memories do not empty simultaneously as in the prior art but rather the cell memories empty sequentially (see Fig. 3). As a result, only 2 ATM cell memories per channel-specific memory are required.

Fig. 3 shows the conditions on the data lines Data_Ch0...Data_Ch3 downstream of the channel-specific memories SP0...SP3. The ATM cells are indicated by header H and payload P. The chronological offset of the transmission is clearly apparent here.

In the exemplary embodiment, the minimization of the ATM cell memories was referred to. However, the invention is not restricted to ATM cells and ATM cell memories. Instead, packets of a general type such as IP packets, for example, can also be removed from packet

memories in accordance with the method according to the invention. As a consequence, the packet memories can then be minimized in the same way as the ATM cell memories of the exemplary embodiment.

Description

Method for minimizing ATM cell memory

The invention relates to a method according to the preamble of patent claim 1.

Contemporary transmission methods are generally divided into transmission methods which transmit information according to a synchronous transfer mode (STM) or asynchronous transfer mode (ATM).

The synchronous transfer mode STM is based on the transmission of information using SDH (synchronous digital hierarchy) transmission technology. Here, the to information is transmitted in transmission frames. These are divided into a control field (SOH, Section Overhead; POH, Path Overhead) and a container field. In the former, control information relating to the connection is transmitted, while in the latter payload data are stored. ATM cells, for example in ATM systems by means of SDH, can also be used here as payload data. Said data must then be inserted into the frame structure at the start of the transmission process (downstream direction) and removed again at the reception end (upstream direction). For example information relating to the security of the transmission, bit errors, line failure, clock accuracy etc. are possible as control information.

The control field has two subregions SOH and POH. The subregion designated by SOH has control information relating to a transmission section (for example between two switching devices), while control information is transmitted between two users (end-to-end) in the subregion which is designated by POH.

In contemporary synchronous transmission methods, STM-1 interfaces are used. An STM-1 interface is represented physically by a connection between two SDH switching devices. The STM-1 interface is thus the basis of the SDH transmission. For this reason, the SDH switching matrices arranged in the SDH switching device are currently configured in the prior art for the switching through of STM-1 signals.

However, in future the intention is for higher-order signals such as STM-N (N>1) signals to be capable of being switched through. Because this is not the case at present, through-switching problems are experienced with the SDH switching matrices which have been used hitherto. A method of avoiding these problems which has been known in the prior art is the virtual concatenated mode. It is a standardized method with which, for example, an STM-4 datastream is split up into 4 STM-1 datastreams. During the transmission, 4 STM-1 datastreams are thus fed to the receiving switch, switched through and then combined again to form an STM-4 datastream. However, for this purpose, the STM-1 datastreams which are transmitted in channels must have a common reference variable so that later recombination can occur.

The non-concatenated mode is to be seen in contrast to the above. Here, the respective signals, for example STM-1 datastreams, are transmitted in channels which are independent of one another.

The standard interface for the transfer of ATM cells in the non-concatenated mode is the Utopia Level 2 interface. ATM cells are received by this interface and written into channel-specific memories in accordance with the assigned channel number. In a first step, it is determined here whether the channel-specific memory in question is free. Only if this is the case is an ATM cell written in.

The ATM cells stored in the channel-specific memories are then received by a framer device and inserted into an SDH frame structure. The ATM cells are thus written at a predefined speed into channel-specific memories and removed again from them with a speed which deviates therefrom. Although the writing-in speed which is predefined by the Utopia Level 2 interface is higher (on average approximately 4 times) than the reading-out speed predefined by the framer device, it is to be borne in mind here that the writing-in process is stopped by the reception of an SOH field. An increase in the reading-out speed of the framer device is thus absolutely necessary. In this case, the Utopia Level 2 interface may no longer be capable of appropriately filling the the FIFO cell memories of each channel-specific memory. As a consequence, empty cells are inserted into the frame structure, which is to be avoided for considerations of dynamics because this prevents a full load from being reached.

In the prior art, a structure in which a total of 4 FIFO cell memories are used per channel-specific memory has become apparent as the solution to this problem. Here, it is necessary to bear in mind that neither the framer device nor the Utopia Level 2 interface can simultaneously access the same FIFO cell memory. At the start, all the FIFO cell memories are filled with ATM cells. In a first step, the framer device simultaneously reads out the ATM cells of in each case one of the 4 FIFO cell memories of all the channel-specific memories. As a result, the Utopia Level 2 interface is indirectly actuated in such a way that the FIFO cell memories which are now emptied are filled again with ATM cells by said interface. The framer device then cyclically reads out the further FIFO cell memories. Because a total of 4 FIFO cell memories are provided per channel-specific memory, care is taken to ensure that one of the 4 FIFO

cell memories per channel-specific memory is always full. The STM-4 interface then operates at full load. The 4 FIFO cell memories per channel-specific memory average the pauses between the different frequencies during the writing and reading processes.

It is problematic here that when there are higher-order interfaces (for example STM-4, STM-16 etc.), the number of FIFO cell memories rises drastically. However, this results in problems not only with the complexity of the entire transmission system (for example increased susceptibility to faults) but also with an increased power drain of the modules in the interfaces and associated warming. Furthermore, it is associated with increased costs (additional silicon costs).

The invention is based on the object of indicating a way in which the number of cell memories for the non-concatenated mode can be reduced.

The invention is achieved on the basis of the features specified in the preamble of patent claim 1 by means of the features claimed in the characterizing part.

An advantage of the invention is in particular the fact that the spatial arrangement of the FIFO cell memories of the prior art is converted, as it were, into a chronological arrangement. This means that, here too, the definition of the Utopia Level 2 interface is taken into account by ensuring that if the reading device accesses an ATM cell memory, an ATM cell is always stored in it, and it is thus not necessary to insert any empty cells into the SDH transmission frame. This is achieved by virtue of the fact that the ATM cells stored in the ATM cell memory are removed from them in a chronologically staggered reading-out process.

Advantageous developments of the invention are specified in the subclaims.

The invention is explained in more detail below with reference to an exemplary embodiment. In the drawing:

Fig. 1 shows the arrangement of the circuit arrangement according to the invention in a communications system,

Fig. 2 shows the circuit arrangement according to the invention,

Fig. 3 shows the conditions on the data lines Data_Ch0… Data_Ch3.

Fig. 1 shows the arrangement of the circuit arrangement according to the invention in a communications system KS. According to said arrangement, a switching matrix SN, which can be used for switching through the ATM cells, is disclosed as a central component of the communications system KS. In addition, ATM port devices P and devices SDH, between which the Utopia Level 2 interface is arranged, are shown. Said interface is simultaneously part of the two devices. The circuit arrangement according to the invention is then integrated into the device SDH. Framer devices (not shown here in more detail) which integrate the ATM cells into SDH transmission frames are to be considered as part of the device SDH. The circuit arrangement according to the invention is located in the downstream direction.

Fig. 2 shows the circuit arrangement according to the invention in detail. According to said arrangement, channel-specific memories SP0…SP3 which each have 2 FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ are disclosed. An FIFO cell memory can hold precisely one ATM cell. 2 FIFO cell memories are necessary because writing/reading

processes cannot be performed simultaneously in one ATM cell memory. Therefore, while one ATM cell is removed from one of the ATM cell memories, a further ATM cell can thus be written into the remaining ATM cell memory.

According to Fig. 2, the channel-specific memory SP0 thus has the two FIFO cell memories $FIFO_{01}$, $FIFO_{02}$, the channel-specific memory SP1 has the two FIFO cell memories $FIFO_{11}$, $FIFO_{12}$ and so on. The channel-specific memories SP0...SP3 are operatively connected to the Utopia Level 2 interface. Said interface receives the ATM cells from the ATM port P and writes them to one of the two FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ of the respective channel-specific memory SP0...SP3 in accordance with the channel Ch0...Ch3. The channel Ch0 is thus assigned the channel-specific memory SP0, and the channel Ch1 is thus assigned the channel-specific memory SP1 etc. The Utopia Level 2 interface must ensure at all times that the ATM cell memories are filled with ATM cells. The reason for this is that otherwise the framer device integrates empty cells into the SDH frames. The ATM cells are written into the channel-specific memories at a speed which is predefined by the Utopia Level 2 interface.

Furthermore, Fig. 2 shows a framer device FR. It removes the ATM cells from one of the two FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ of the respective channel-specific memory SP0...SP3 and integrates them into SDH transmission frames. The reading-out processes are supported by a reading counter RC which controls the chronological sequencing of the reading-out processes by means of devices RC0...RC3. The ATM cells are removed from the respective channel-specific memories SP0...SP3 again at a speed which differs from the writing-in speed and is predefined by the framer device FR.

In order to aim at transmission of the greatest possible efficiency, the Utopia Level 2 interface must fill up the channel-specific memories SP0...SP3 with ATM cells, and the framer device FR must correspondingly read out the ATM cells, in such a way that the dwell time of the ATM cells in the FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ is as short as possible. For this purpose, the writing/reading processes have to be correspondingly matched to one another.

For this purpose, the writing/reading process is started from an initial state. In this state, all the FIFO cell memories $FIFO_{xy}$, $FIFO_{xz}$ are to be filled with ATM cells. The Utopia Level 2 interface thus writes no ATM cells into the channel-specific memories SP0...SP3. The framer device FR initially reads out an ATM cell from the ATM cell memory $FIFO_{01}$ of the channel-specific memory SP0 byte by byte. The decisive factor here is the counter reading of the counting device RC0. The counter reading results from the counting device RC being acted on by an offset. In the present case, this offset is 0 bytes.

The counter reading of the counting device RC1 then specifies when the ATM cell stored in the ATM cell memory $FIFO_{11}$ of the channel-specific memory SP1 is to be read out. The counter reading results from the counting device RC being acted on by a further offset. In the present case, this is 13 bytes. This means that the reading out of the ATM cell stored in the cell memory $FIFO_{11}$ is not started until 13 bytes of the ATM cell of the ATM cell memory $FIFO_{01}$ have been read out. The offsets of the counting devices RC2 and RC3 are 26 and 39 bytes. The reading out takes place cyclically. During the reading-out processes, the Utopia Level 2 interface can write further ATM cells into the ATM cell memories. The criterion for this is, however, that the respective ATM cell memory is empty. As a result of

this method, 4 cell memories do not empty simultaneously as in the prior art but rather the cell memories empty sequentially (see Fig. 3). As a result, only 2 ATM cell memories per channel-specific memory are required.

Fig. 3 shows the conditions on the data lines Data_Ch0...Data_Ch3 downstream of the channel-specific memories SP0...SP3. The ATM cells are indicated by header H and payload P. The chronological offset of the transmission is clearly apparent here.

In the exemplary embodiment, the minimization of the ATM cell memories was referred to. However, the invention is not restricted to ATM cells and ATM cell memories. Instead, packets of a general type such as IP packets, for example, can also be removed from packet memories in accordance with the method according to the invention. As a consequence, the packet memories can then be minimized in the same way as the ATM cell memories of the exemplary embodiment.

Patent claims

1. A method for minimizing packet memory, having a multiplicity of channel-specific packet memories ($FIFO_{xy}$, $FIFO_{xz}$), each of which can be used to hold a data packet, the data packets being read into a channel-specific packet memory by a writing device (Utopia Level 2) and removed from it again by a reading device (FR), characterized in that the data packets stored in the multiplicity of channel-specific packet memories ($FIFO_{xy}$, $FIFO_{xz}$) are read out cyclically under the control of the reading device (FR) in accordance with the status of a multiplicity of counting devices (RC0...RCn).

2. The method as claimed in claim 1, characterized in that the multiplicity of counting devices (RC0..RCn) is embodied in such a way that each of these counting devices is assigned in each case to one of the channel-specific packet memories ($FIFO_{xy}$, $FIFO_{xz}$).

3. The method as claimed in claim 1, 2, characterized in that the status of two counting devices (RC0...RCn) differs essentially by a factor which is distinguished from the division of the number of bytes of a data packet (for example 53) and the number of channels.

4. The method as claimed in claim 1 to 3, characterized in that the data packets are embodied as ATM cells, and the packet memories are embodied as ATM cell memories ($FIFO_{xy}$, $FIFO_{xz}$).

5. The method as claimed in claim 1 to 4, characterized in that the writing device is embodied as a Utopia Level 2 interface.

6. The method as claimed in claim 1 to 4, characterized in that the reading device is embodied as

a framer device (FR) which inserts ATM cells into an SDH transmission frame.

10/088140

Abstract

Method for minimizing ATM cell memory

In the prior art, ATM cells are converted into STM-4 signals as STM-1 datastreams via the Utopia Level 2 interface in the non-concatenated mode, for example for the STM-4 interface. For this purpose, 4 ATM cell memories, which are necessary owing to the specifications of this interface, are required for each channel. In order to reduce this number, the ATM cells are removed from the ATM cell memories with a chronological offset. As a result, the number of ATM cell memories can be halved without restrictions having to be accepted in the transmission process.

Fig. 2

FIG 1

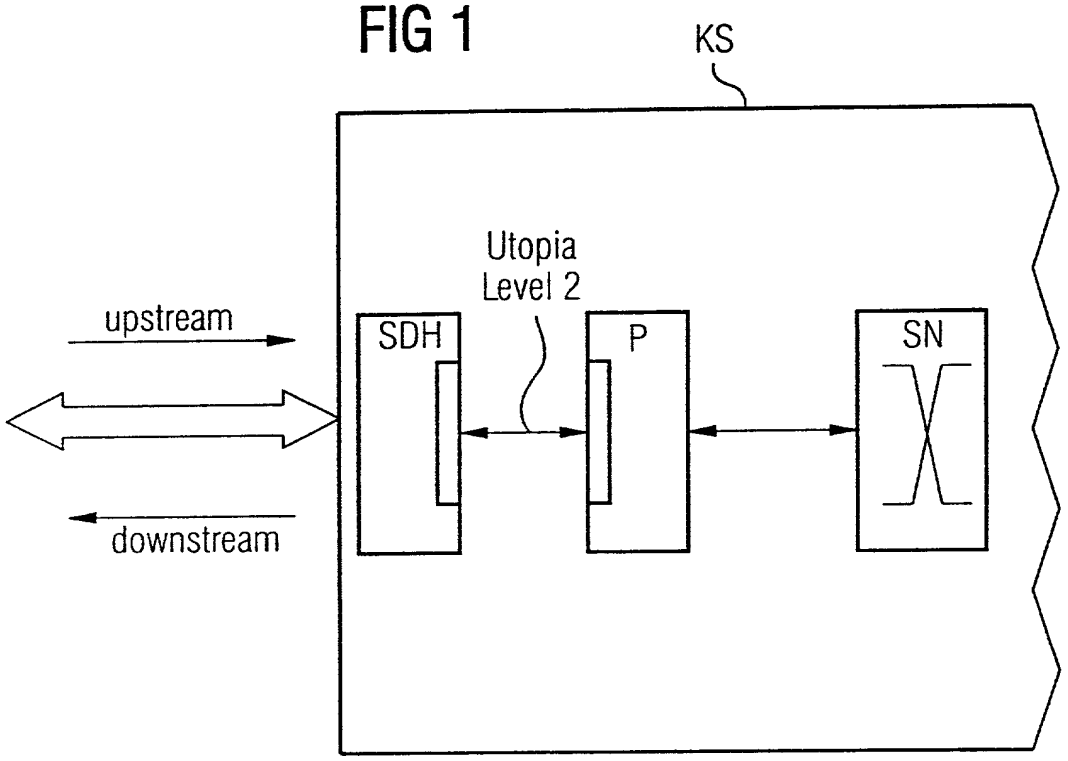
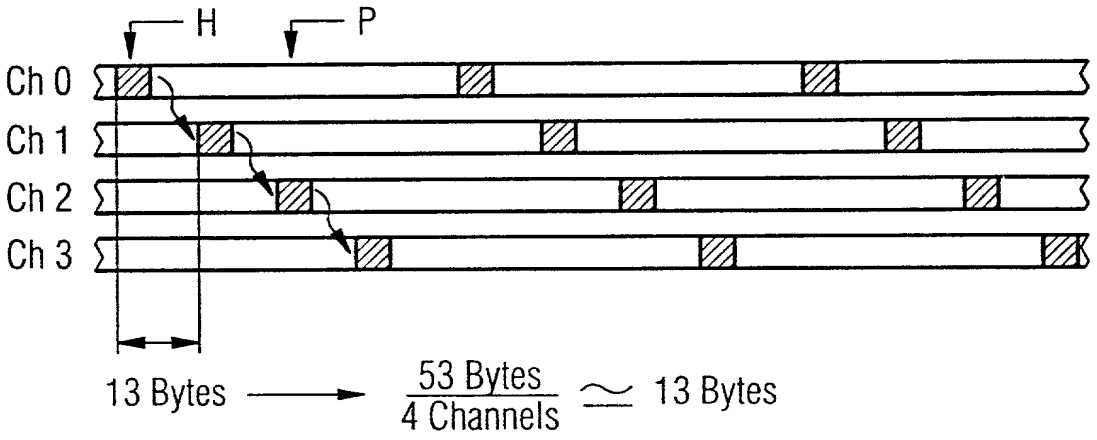

KS
Utopia
Level 2
upstream
SDH
P
SN
downstream

FIG 3


H
P
Ch 0
Ch 1
Ch 2
Ch 3
13 Bytes
53 Bytes
4 Channels
13 Bytes

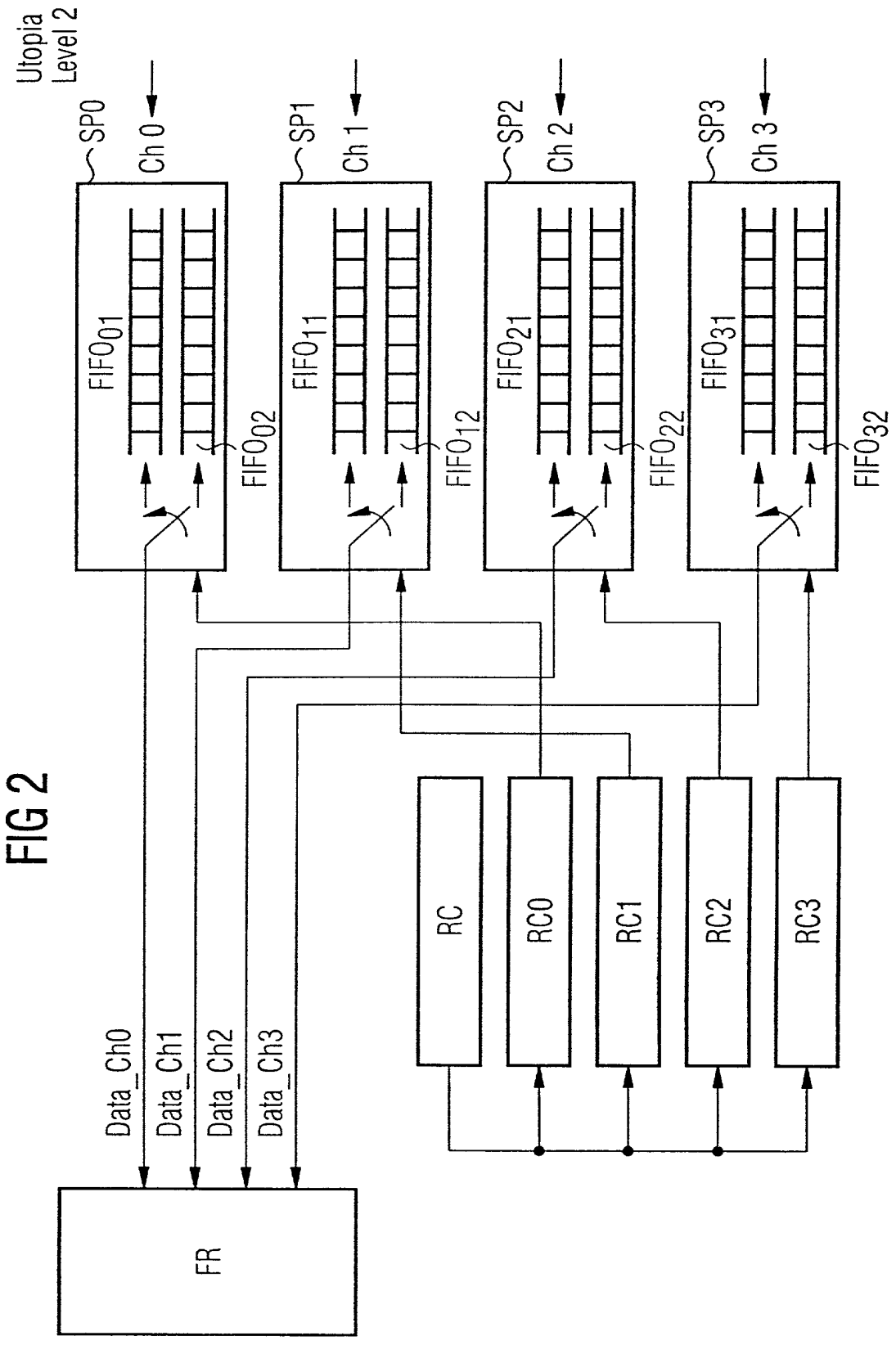


FIG 2

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Verfahren zum Minimieren von ATM-Zellenspeicher

Method for minimising ATM cell memories

deren Beschreibung

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 25.07.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE00/02441
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

the specification of which

(check one)
☐ is attached hereto.
☒ was filed on 25.07.2000 as
PCT international application
PCT Application No. PCT/DE00/02441
and was amended on _____
(if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
19944490.0	DE	16.09.1999	☒	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein
			☐	☐
(Number)	(Country)	(Day Month Year Filed)	Yes	No
(Nummer)	(Land)	(Tag Monat Jahr eingereicht)	Ja	Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/02441	25.07.2000	anhängig	pending
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D, M, Y) (Anmeldedatum T, M, J)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

Customer No. 25227

Telefongespräche bitte richten an:
(Name und Telefonnummer)

Direct Telephone Calls to: *(name and telephone number)*

Ext. _____

Postanschrift:

Send Correspondence to:

Morrison and Foerster LLP
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Telephone: (001) 202 887 1500 and Facsimile (001) 202 887 0763
or
Customer No. 25227

Voller Name des einzigen oder ursprünglichen Erfinders:	Full name of sole or first inventor:
Athanase Mariggis	Athanase Mariggis
Unterschrift des Erfinders Datum Athanase Mariggis (Mariggis) 25.1.02	Inventor's signature Date
Wohnsitz Muenchen, DEUTSCHLAND DEX	Residence Muenchen, GERMANY
Staatsangehörigkeit GR	Citizenship GR
Postanschrift Schuckertstr. 1 81379 Muenchen	Post Office Addess Schuckertstr. 1 81379 Muenchen
Voller Name des zweiten Miterfinders (falls zutreffend):	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz ,	Residence ,
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).